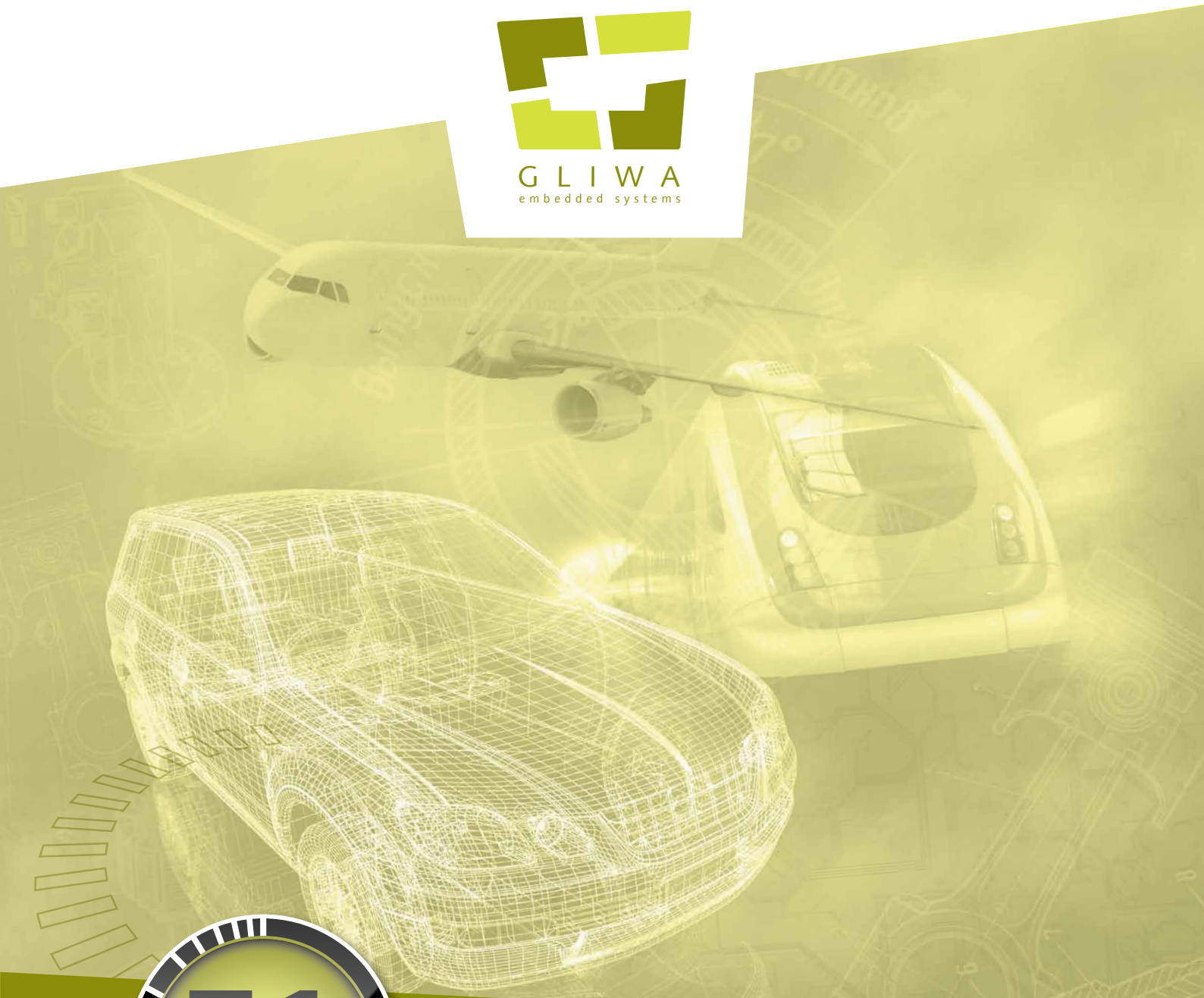
WE DEVELOP PRECISION

GLIWA
embedded systems



T1

TIMING 1st CLASS

TIMING SUITE FOR REAL-TIME SYSTEMS

TIMING 1st CLASS

T1 - THE COMPREHENSIVE SOLUTION FOR RUN-TIME SYSTEMS

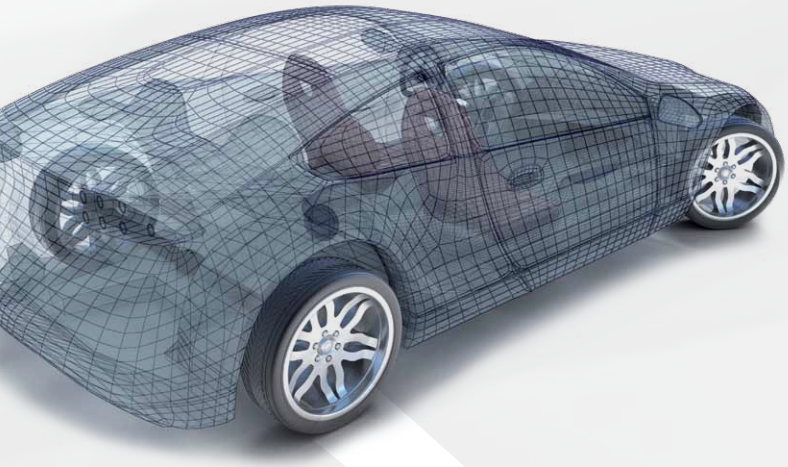
T1 is the most comprehensive timing suite for the analysis of run-time properties of real-time systems. The sophisticated representation makes complex software behaviours easy to understand. Support for timing debugging is optimal. The delivery of diverse timing parameters allows a highly detailed analysis. As required, evaluation of results can be performed by T1 components on the target system. Thus, T1 performs not only pure measurements but also high-level timing analysis. Timing constraints can be continually monitored and any violations are then clearly identified.

T1 GROWS WITH YOUR NEEDS

Many software releases arise up until delivery of a production ECU. Additions and changes are commonplace. T1 accompanies the system analysis from the start and highlights bottlenecks early in the development process. The consequence is an optimisation process that will be your partner through every phase of the project.

FROM PROTOTYPE TO PRODUCTION ECU

T1 is wherever you need it. Whether starting with module tests and then progressing to the automated test environment (e.g. HIL) or in the finished ECU, T1 produces exact execution time measurements in each phase of the project, even in the production ECU. In this way, measurement data can be obtained, for example via CAN, with very modest demands on the transfer bandwidth.



ANALYSIS AND UNDERSTANDING OF RUN-TIMES

T1 grants insights into the system. Sequences are made visible and easy to understand. Timing problems are recognised in time and solved using the visualisation.

T1 IS MODULAR

T1 is composed of various components and provides the users with diverse analysis tools. As the complexity and analysis tasks grow, so T1 grows with them. In this way, key development milestones are verified. Delivery delays due to timing problems are prevented by T1.

OPTIMISATION

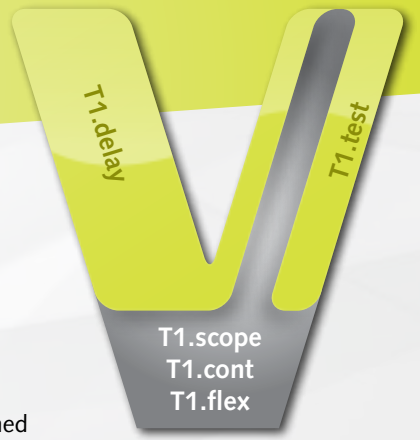
It is quite common to find that a functionally perfect design suffers, in spite of enormous CPU reserves, timing failures. T1 immediately shows where to start. During the repair of an overloaded system, T1 helps to find optimisation opportunities and to evaluate all changes.

DEBUGGING

Experience has shown that, as a rule, the investigation of timing problems start in the wrong place, with the functional behaviour. Cause and effect of a timing problem are often far apart. “Digging around” with a debugger can consume weeks. T1 brings about a drastic reduction in the time required to solve timing problems.

DOCUMENTATION

Standards such as ISO 26262 or DO 178-B/C require clear and thorough documentation. T1 produces fully automatic reports of timing behaviour on demand. Once configured, the required documents can be obtained at the press of a button.



T1 ENSURES "SOP" FOR PRODUCTION ECUs

T1 assists with all phases of timing verification. T1 is particularly renowned for its value in the integration phase of production ECUS, when various software components come together and the system is on the test bed.

T1 INTEGRATION IN A CUSTOMER PROJECT

Leaving nothing to chance, GLIWA GmbH integrates T1 on site with the customer:

- **T1-Adaption:** T1 is adapted as required, for processor, RTOS, compiler and interface. Many variants are available "out of the box" (see datasheet on reverse).
- **T1-Integration:** T1 is directly integrated into the customer project. The team of GLIWA experts supply engineering services to achieve this integration. This provides the customer with a guaranteed Plug & Play.
- **T1-Usage:** T1 measurements are made from now on.

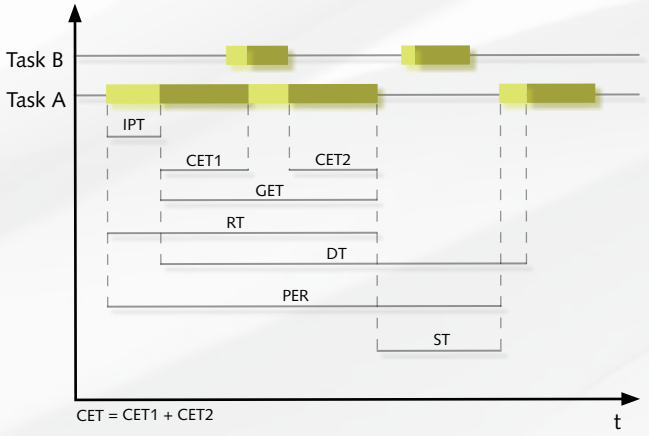
T1 DEPLOYMENT IN MULTIPROCESSOR SYSTEMS

T1 is already installed in system with several cores. This applies to systems with several CPUs as well as multi-core architectures.
T1 is being continually developed with new features for multi-core systems.

PROPERTIES MEASURED BY T1

This table gives an overview of
the most used values in the field of timing analysis:

ABREVIATION	DESCRIPTION
IPT	*initial pending time*
CET	*core execution time*
GET	*gross execution time*
RT	*response time*
DT	*delta time*
PER	*period*
ST	*slack time*
CPU	*CPU load*
JIT	*jitter*



DATASHEET

BASIC FUNCTIONS

Project explorer	*2 views, system and application view, incl. code viewer*
Project import	*Source, object code such as ELF files with debug info*
HTML reports	*Reports of all timing info with images in chosen font / colour*
CSV reports	*CSV reports formatted Ws, XXms, YYus, ZZns, times: ns, µs, ms, s*
Report configuration	*Freely configurable, incl. summary with graphic*
Save report	*Yes, projects and configurations in T1 project files*
Symbol resolver	*Extracted from addresses, symbols and debug information*
Symbol search	*Search for any symbol*
ELF info dialogue	*Dialogue box for ELF file data*
Connection logger	*Logs all T1 CAN messages (RX and TX)*
Send traces	*Compress all data into a Zip archive in an email*

THE SW OSCILLOSCOPE

T1.scope is the basic component. As with an oscilloscope display, the timing of tasks is graphically represented on the time axis. Incidences of interrupts or arbitrary events are visualised in the same way. The focus of the measurement can be freely configured.

The supervision of access to particular data is equally possible. With simple mouse gestures, regions can be selected and analysed. The data is prepared in the background and collected together with relevant results. T1.scope offers many additional functions.

Measurement results can be exported as HTML files, for example, and communicated to project partners by email for graphical and quantitative evaluation.

FUNCTIONS

Generic	*Synchronised views with auto-update across various windows*
Trace view (basic functions)	*Graphical representation of timing events with scheduling, stopwatches and data flows, user events, constraints and highlighting of constraint violations, overhead measurement, min and max values, CPU load diagram, comments/ bookmarks, CPU load for tasks and for the entire system, user time grids*
Trace view (Additional functions)	*Zoom, mark, scale, select, Look & Feel, various tree representations etc.*
Save & Print	*Binary trace format, text traces all with additional information*
Measured values	*CET, GET, IPT, RT, DT, PER, ST, PRE, JIT, CPU-Load, occurance*
Charts	*Pie chart, histograms, bar charts, statistical representation incl. extrapolated values*
Corrections	*Corrections and compensation for measurement overhead*
Trigger	*Trigger measurement of desired intervals*
Trace download	*Permanent or selective trace download*

ALWAYS UP-TO-DATE WITH T1

T1 is being continually developed to meet evolving customer needs**.** This datasheet is just an overview. T1 can generally be integrated into any environment (CPU, RTOS, tool environment, hardware interface etc.).

HIGHLY FLEXIBLE ON-TARGET TIMING MEASUREMENT

T1.flex is, among other things, the tool of choice for completely unexpected effects, allowing instrumentation to be inserted at run-time. This allows code timing measurements to be performed without having instrumented in advance. This means that the software does not have to be recompiled or flashed!

T1.flex exploits special features of the controller and its hardware architecture. When timing problems emerge, such ad hoc measurement results can be generated. This process makes T1 a powerful and highly flexible analysis system that proves itself most valuable at the most critical phases of your project.

FUNCTIONS

SWF	*Stopwatch on function, also as a focus measurement*
SWC	*Stopwatch on code segment, also as a focus measurement*
CAF	*Code access frequency*
DAF	*Data access frequency*
DAF mit RMC/RMF	*Data access frequency with restriction to code segment or function*
UED	*User event on data, user event on access to data*
UED mit RMC/RMF	*User event on data with restriction to code segment or function*
UEC	*User event on code access,*
Symbol groups	*Configure symbol groups*
Address range	*Start-end region, code addr., symbol name, source code region, …*
STA	*Set stop trigger on access to code or data*
STA immediate	*Directly set a stop trigger to a specific address*
NCA	*next code access, report jump destinations*
CPC	*Code path counter, for example for loop bound analysis*
Other	*Source viewer, save, flexible stopwatches, flexible configuration and more*

FUNCTIONAL WILDCARDS

In the lifecycle of a project, function groups emerge sequentially. With T1.delay, users can load the CPU using delays in place of the missing functions. In this way, system timing can be estimated before the functional code is fully available. For large project groups, in particular, and for collaboration with suppliers, T1.delay becomes an indispensable cornerstone of planning.

FUNCTIONS	
Delay function	*Produces artificial delay and represents place-holder for function code yet to be added*
Auto-increment	*Delay can be automatically incremented. This allows empirical boundaries to be determined*
Reset DLY	*Reset DeLaY resets the delay function*

T1 test

VERIFICATION AT THE SYSTEM AND CODE LEVEL

T1.test provides fully automatic timing measurement. The integration with the test environment is achieved using XML scripts via the .NET, .exe or Python interface. The deployment of timing verification in functional tests (e.g. HIL) is particularly efficient. In this way, both functional and timing properties can be verified at the same time. T1 also generates the appropriate documentation of the timing analysis.

FUNCTIONS	
Start T1	*Starts T1 from an external Tool*
Start T1 script	*Starts a T1 script from an external tool*
Stop T1	*Stops T1 from an external tool*
Auto-log	*Generates a log file recording the automation for documentation*

Overview of automated commands (excerpt):
Connection start/stop, start/stop measurement, auto-download (permanent, wait for trigger, stop), HTML or CSV report generation, load project, trace load/save, configure/update delays, reset/start/stop delay increment, set directory (for load/save), constraint check, set application feature mask, perform T1.flex measurements (SWF, SWC, CAF or DAF), measurement of symbol groups with or without focus.

T1 cont

CONTINUAL ON-TARGET TIMING ANALYSIS

In contrast to T1.scope, **T1.cont performs calculations on the target**, an ideal process for timing measurement over long durations. All tasks and interrupts are included. Minimum and maximum timing values can be continuously collected and, using "focus measurements" also average (mean) values. Optional constraints permit the early detection of violations of freely definable limits. A constraint violation triggers a T1.scope visualisation and/or a user-defined callback function. Using a callback, the application can take exactly the appropriate measures, such as recording the problem in the error log. In this way, even timing problems can be uncovered with minimal effort, even when they occur only rarely in long tests.

FUNCTIONS	
Results	*CET, GET, IPT, RT, DT, ST, CPU-Load*
Stopwatches	*Continual min/max CET/GET also dynamic T1.flex Stopwatches*
Dynamic configuration	*Online reconfiguration of computation values, results, supervised constraints*
Data presentation	*graphical or tabular results presentation*
Save / Load	*T1.cont trace data for further analysis*
Focus measurement	*Focus on specific timing values and defined intervals*
Focus groups	*Focus measurement groups of elements, such as all tasks, ISRs, etc.*
Reset	*Reset results*
Constraint On/Off	*Targetted On/Off of the constraint*
Analysis On/Off	*Targetted On/Off of event analysis and computation*
Live status	*Live status monitoring with the GUI*

PORTS / INTERFACES

CONTROLLER

Supplier	*Core*	*Controller*	*Remarks*
Atmel	*AVR MEGA*	*ATmega32, ...*	*T1.flex not yet available*
Atmel	*AVR XMEGA*	*ATxmega32, ...*	*T1.flex not yet available*
Freescale	*CPU12/CPU12X*	*HC12/S12/S12X*	*T1.flex not yet available*
Freescale	*e200*	*MPC5xxx*	*full support*
Freescale	*Power Architektur*	*MPC5xx*	*full support*
Fujitsu	*F²MC-16*	*F²MC-16*	*T1.flex not yet available*
Infineon	*TriCore 1.3.1*	*TC1797, ...*	*full support*
Infineon	*TriCore 1.6*	*TC1798, ...*	*full support*
Infineon	*TriCore, AURIX*	*MultiCore*	*full support*
Infineon	*C166 v1/2*	*(X)C16x / ST10*	*full support*
Microchip	*dsPIC*	*dsPIC33FJ, ...*	*T1.flex not yet available*
NXP	*Cortex M0*	*LPC11xx*	*T1.flex not yet available*
NXP	*Cortex M3*	*LPC17xx*	*full support*
Renesas	*V850e1 / e2 (dual)*	*V850, PX4,...*	*full support*
Texas Instr.	*Cortex M3*	*TMS570*	*full support*
Texas Instr.	*Cortex R4*	*TMS570*	*full support*

RTOS

Supplier	*Name*	*Supplier*	*Name*
GLIWA GmbH	*gliwOS*	**Elektrobit**	*ProOSEK, OEKtime*
ETAS	*ERCOSEK*	**Elektrobit**	*tresOS*
vector	*osCAN*	**ETAS**	*RTA-OSEK*
Delphi	*PharOS*	**KPIT Cummins**	*KPIT*
Micrium	*µC/OS-II*	**Custom OS**	*multiple*

COMPILER

Supplier	*Compiler*	*Core*
Altium	*Tasking*	*C166 and TriCore*
Atmel	*AVR/(X)MEGA*	*AVR (X)MEGA*
Freescale	*Metrowerks*	*CPU12(X), power archit. and e200*
Fujitsu	*Softune*	*F²M-16*
GNU	*gcc*	*TriCore, (X)MEGA, ARM Cortex M0/M3, dsPIC*
Green Hills Software	*GHS Compiler*	*e200, V850e1/e2*
Texas Instruments	*TI Compiler*	*ARM Cortex M3, ARM Cortex R4*

FILE FORMAT IMPORT/EXPORT

Type	*Description*
binary	*Timing and trace data*
txt	*Trace data*
csv	*Timing and trace data*
html	*Timing data, system configuration*
ATF	*ALL-TIMES timing data (based on EU ALL-TIMES project)*
CTF	*Common Timing Format, comprehensive platform*
OT1	*Open Timing Format*
elf	*ELF (Executable and Linkable Format)*
XTC	*Interface to the AbsInt tool suite aiT*
SymTA/S XML	*Interface to the Symtavision tool suite SymTA/S*
INCHRON XML	*Interface to the INCHRON tool suite*
T1 script	*Timing and trace data*
Artop	*Interface to ARTime*

AUTOSAR

Gliwa GmbH is an AUTOSAR development member

Gliwa GmbH possesses years of experience
in the optimisation of timing properties.
Many customers already profit from coaching projects.
In this way, valuable know-how
is introduced into the organisation.

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